16-Bit Parallel BCH(8176, 8072) Encoder

Features

- **16-bit parallel input and 16-bit parallel output**
- **Available for FPGA or ASIC implementation**
- **High speed design, reaches 3.7 Gbps data rate in Virtex IV, higher in ASIC**
- **Compact design, uses 574 CLB slices in Virtex IV, among the smallest on the market**
- **Can work continuously with no gap between code blocks**
- **Fully synchronous one clock design**
- **4 clock cycle latency**

Functional Description

The block diagram of the encoder is shown in Figure 1. The major functional block of the encoder is the parity unit. While the encoder outputs the data symbol, the parity unit calculates the parity symbol at the same time. The parity symbols are appended at the end of the data block to form the whole code word.

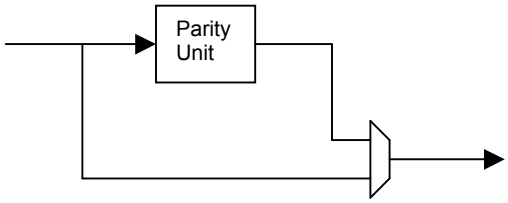

Figure 1. Block diagram of the Reed-Solomon encoder.

Pin Out

Figure 2 is the schematic symbol of the Reed-Solomon encoder.

RST
One bit input, the asynchronous reset. When RST is set high, all the internal flip-flops are asynchronously initialized. The core will stay in this state until RST is set low.

CLK
One bit input, the global clock. All sequential logic acts on the rising edge of CLK.

START
One bit input, the signal to start the encoding process. At the rising edge of CLK, if START is high while RST is low, the internal state machine will start the encoding process. For continuous operation, the START signal for the next code block must line up with the last parity byte of the previous code block. Otherwise, the START signal for the next code block must be at least five clocks after the last parity byte of the previous code block for the decoder to correctly decode the second code word. The length of START should be one clock cycle.

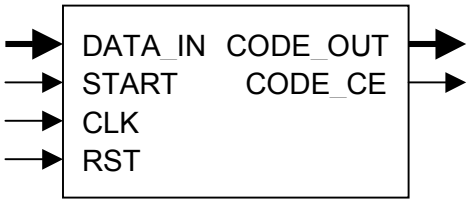

Figure 2. Schematic symbol of the decoder

DATA_IN
Sixteen bit input, the data sequence to be encoded. The first 16-bit symbol of the data sequence should be one clock after the START pulse. The encoder reads in one 16-bit symbol every clock. Each data sequence must have 28 16-bit symbols. Since the data block has only 444 bits, only the 12 MSBs of the 28 16-bit symbol are used as data bits. The encoder will append 36 parity check bits at the end of the data sequence and the output of the encoder is 30 16-bit symbols. For continuous operation there must be 3 clock cycles gap between consecutive data blocks. Otherwise, the gap must be at least nine clock cycles.

CODE_OUT

Sixteen bit output, the output code word. It contains 30 16-bit symbols.

CODE_CE
One bit output, the clock enable for outputting the code word. The length of CODE_CE is 30 clock cycles.

Timing Diagrams

The BCH encoder is very easy to be integrated into a larger design. The following timing diagrams help to clarify some of the synchronization issues.

Figure 3 shows the timing diagram at the starting point of the encoding process, where D0 is the first 16-bit symbol of the data sequence.

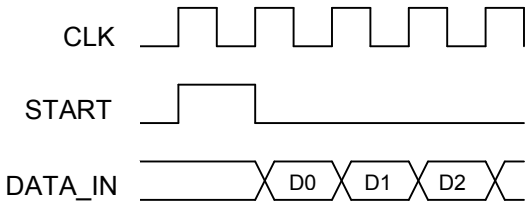

Figure 3. The timing diagram at the starting point of the encoding process

Figure 4 shows the timing diagram at the starting point of the output, where C0 is the first 16-bit symbol of the code word.

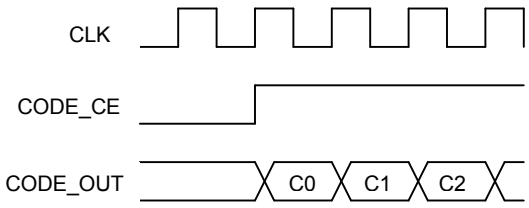

Figure 4. The timing diagram at the starting point of the output

Figure 5 shows the timing diagram of the continuous operation mode, where DA29 is the last 16-bit parity symbol of the first code word and DB0 is the first 16-bit symbol of the following data sequence word.

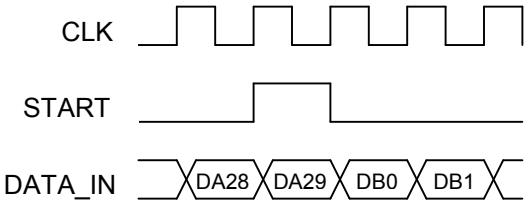

Figure 5. The timing diagram of the continuous operation mode

Deliverables

Deliverables include the encoder and the test bench. For Xilinx or Altera FPGA implementation, both source code and netlist are available. For ASIC implementation, only source code will be delivered. Source code can be in VHDL or Verilog.

Ordering Information

We have flexible licensing structures. Please use the following information to contact us:

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