# DVB_S2 BCH Code Decoder

## Features

- **Flexible BCH decoder. Fully compliant with the DVB_S2 standard. Supports all the code lengths and data lengths defined in the standard.**
- **Available for Xilinx FPGA or ASIC implementation**
- **High speed design, maximum clock speed reaches 80 MHz in Virtex-II**
- **Compact design, uses 5801 CLB slices and 10 block RAMs in Virtex-II**
- **Code length + 2 * (t^2) + 8 * t + 12 clock cycle latency**

## Functional Description

The BCH decoder has three functional blocks and one memory block as shown in Figure 1. First the syndrome unit calculates the syndromes. Then the key equation solver solves the key equation for the error location polynomial. The correction unit calculates the error location and generates the error sequence. The memory unit is used to store the received code word while the decoder calculates the syndromes and solves the key equation. During the correction stage, the stored code word is read out from the memory and added to the error sequence to get the corrected code word.

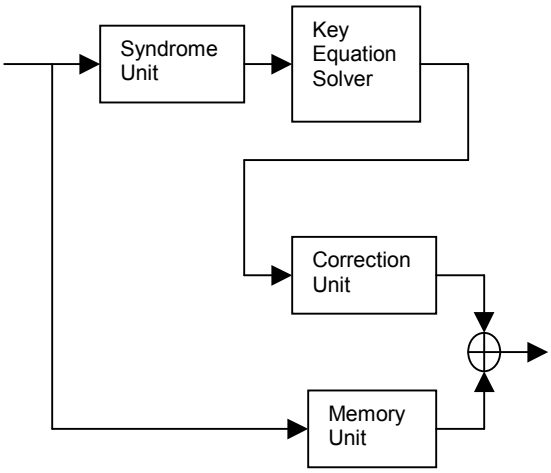


Figure 1. Block diagram of the BCH decoder.

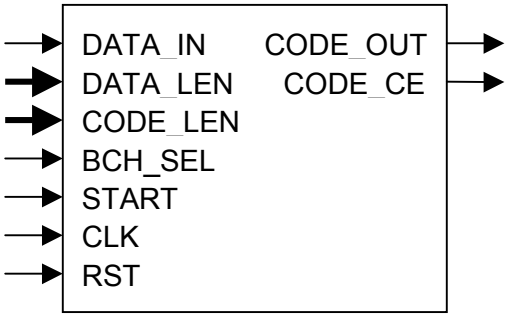


Figure 2. Schematic symbol of the decoder

## Pin Out

Figure 2 is the schematic symbol of the BCH decoder.

### RST

One bit input, the asynchronous reset. When RST is set high, all the internal flip-flops are asynchronously initialized. The core will stay in this state until RST is set low.

### CLK

One bit input, the global clock. All sequential logic acts on the rising edge of CLK.

### START

One bit input, the signal to start the decoding process. At the rising edge of CLK, if START is high while RST is low, the internal state machine will start the decoding process. The length of START should be one clock cycle. .

### BCH_SEL

One bit input, the signal to select either the normal BCH codes or the short BCH codes defined in the DVB_S2 standard. When BCH_SEL = 0, the encoder supports all the normal BCH codes. When BCH_SEL = 1, the encoder supports all the short BCH codes.

CODE_LEN
Sixteen bit input, the code length. All the code lengths defined in the DVB_S2 are supported.

DATA_LEN
Sixteen bit input, the data length. All the code lengths defined in the DVB_S2 are supported.

DATA_IN
One bit input, the received code word. The first bit of the code word should be one clock after the START pulse. The decoder reads in one bit every clock.

CODE_OUT
One bit output, the decoded code word. If the number of erroneous bits is less than or equal to half the number of the parity check bits, the output is the corrected code word. Otherwise, the output is unpredictable.

CODE_CE
One bit output, the clock enable for outputting the corrected code word. The length of CODE_CE is CODE_LEN clock cycles.

## Timing Diagrams

The BCH decoder is very easy to be integrated into a larger design. The following timing diagrams help to clarify some of the synchronization issues.

Figure 3 shows the timing diagram at the starting point of the decoding process, where D0 is the first bit of the received code word.

Figure 4 shows the timing diagram at the starting point of the output, where C0 is the first bit of the decoded code word.

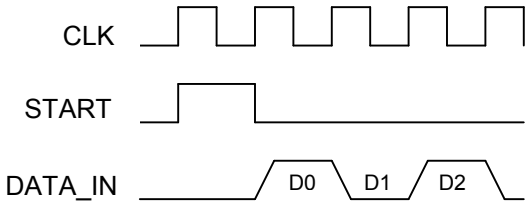


Figure 3. The timing diagram at the starting point of the decoding process

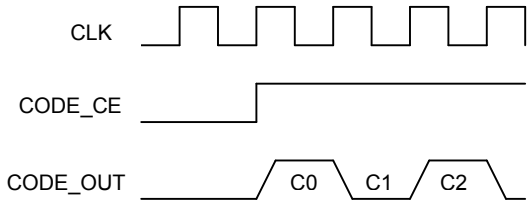


Figure 4. The timing diagram at the starting point of the output

## Deliverables

Deliverables include the encoder/decoder and the test bench. A design document is also included in the deliverable. For Xilinx FPGA implementation, both source code and netlists are available. For ASIC implementation, only source code will be delivered. Source code can be in VHDL or Verilog. A C source code model is also delivered with a source code license.

## Ordering Information

We have flexible licensing structures. Please use the following information to contact us:

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