DVB_S2 BCH Code Encoder

Features

- **Flexible BCH encoder. Fully compliant with the DVB_S2 standard. Supports all the code lengths and data lengths defined in the standard.**
- **Available for Xilinx FPGA or ASIC implementation**
- **High speed design, maximum clock speed reaches 169 MHz in Virtex-II**
- **Compact design, uses 161 CLB slices in Virtex-II**
- **One clock cycle latency**

Functional Description

The block diagram of the encoder is shown in Figure 1. The major functional block of the encoder is the parity unit. While the encoder outputs the data bit, the parity unit calculates the parity bit at the same time. The parity bits are appended at the end of the data block to form the whole code word.

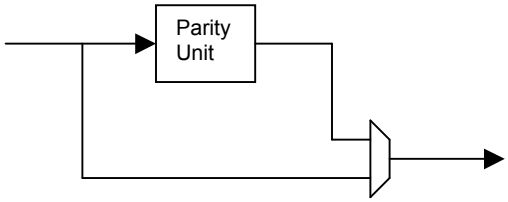

Figure 1. Block diagram of the BCH encoder.

Pin Out

Figure 2 is the schematic symbol of the BCH code encoder.

RST
One bit input, the asynchronous reset. When RST is set high, all the internal flip-flops are asynchronously initialized. The core will stay in this state until RST is set low.

CLK
One bit input, the global clock. All sequential logic acts on the rising edge of CLK.

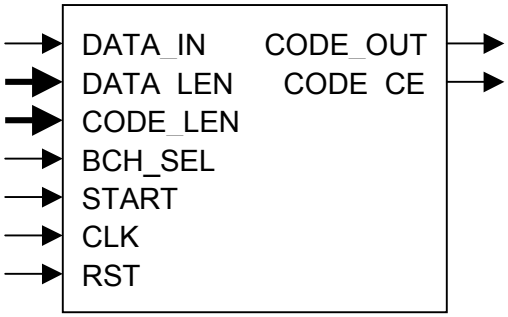

Figure 2. Schematic symbol of the encoder

START
One bit input, the signal to start the encoding process. At the rising edge of CLK, if START is high while RST is low, the internal state machine will start the encoding process. The length of START should be one clock cycle.

BCH_SEL
One bit input, the signal to select either the normal BCH codes or the short BCH codes defined in the DVB_S2 standard. When BCH_SEL = 0, the encoder supports all the normal BCH codes. When BCH_SEL = 1, the encoder supports all the short BCH codes.

CODE_LEN
Sixteen bit input, the code length. All the code lengths defined in the DVB_S2 are supported.

DATA_LEN
Sixteen bit input, the data length. All the data lengths defined in the DVB_S2 standard are supported.

DATA_IN
One bit input, the data sequence to be encoded. The first bit of the data sequence should be one clock after the START pulse. The encoder reads in one bit every clock.

CODE_OUT
One bit output, the output code word. The first part of the code word is the data bits and the second part is the parity check bits.

CODE_CE
One bit output, the clock enable for outputting the code word. The length of CODE_CE equals CODE_LEN clock cycles.

Timing Diagrams

The BCH encoder is very easy to be integrated into a larger design. The following timing diagrams help to clarify some of the synchronization issues.

Figure 3 shows the timing diagram at the starting point of the encoding process, where D0 is the first bit of the data sequence.

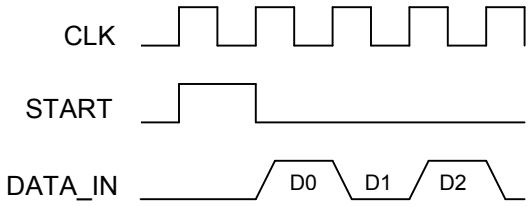

Figure 3. The timing diagram at the starting point of the encoding process

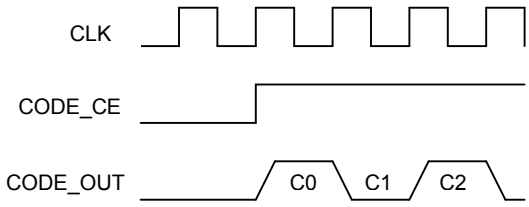

Figure 4. The timing diagram at the starting point of the output

Figure 4 shows the timing diagram at the starting point of the output, where C0 is the first bit of the code word.

Deliverables

Deliverables include the encoder/decoder and the test bench. A design document is also included in the deliverable. For Xilinx FPGA implementation, both source code and netlists are available. For ASIC implementation, only source code will be delivered. Source code can be in VHDL or Verilog. A C source code model is also delivered with a source code license.

Ordering Information

We have flexible licensing structures. Please use the following information to contact us:

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