2.5 Gbps GPON FEC Encoder

Features

- **Fully compliant with the GPON standard (G.984.3), supports 8-bit, 16-bit or 32-bit input for different data rates, supports short last code word**
- **Available for FPGA or ASIC implementation**
- **High speed design, reaches 4.8 Gbps data rate in Virtex II, or 4.0 Gbps data rate in Spartan III, higher in ASIC**
- **Compact design, uses 1363 CLB slices in Virtex II, or 1341 CLB slices in Spartan III**
- **Fully synchronous one clock design**
- **263 clock cycle latency**

Functional Description

The GPON standard uses the (255, 239) Reed-Solomon code as its FEC code. The block diagram of the encoder is shown in Figure 1. The major functional block of the encoder is the parity unit. While the encoder outputs the data symbol, the parity unit calculates the parity symbol at the same time. The parity symbols are appended at the end of the data block to form the whole code word.

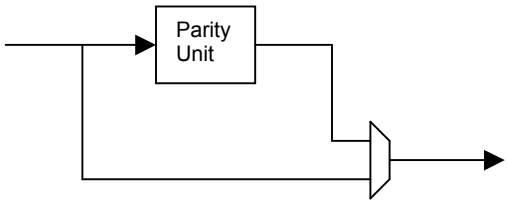

Figure 1. Block diagram of the Reed-Solomon encoder.

Pin Out

Figure 2 is the schematic symbol of the encoder. The pins are explained as follows.

RST
One bit input, the asynchronous reset. When RST is set high, all the internal flip-flops are asynchronously initialized. The core will stay in this state until RST is set low.

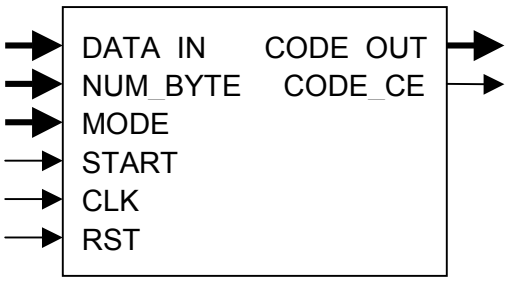

Figure 2. Schematic symbol of the encoder

CLK
One bit input, the global clock. All sequential logic acts on the rising edge of CLK.

START
One bit input, the signal to start the encoding process. At the rising edge of CLK, if START is high while RST is low, the internal state machine will start the encoding process.

MODE
Two bit input. When mode is set to “00”, the 8 msb of DATA_IN is the input and the 8 msb of CODE_OUT is the output. When mode is set to “01”, the 16 msb of DATA_IN is the input and the 16 msb of CODE_OUT is the output. When mode is set to “10” or “11”, the full 32 bit DATA_IN is the input and the full 32 bit CODE_OUT is the output.

NUM_BYTE
Sixteen bit input to specify the number of data bytes to be encoded. NUM_BYTE does not include the added parity bytes. The minimum number of data bytes supported is 1 byte for 8 bit input, 2 bytes for 16 bit input, and 4 bytes for 32 bit input. The highest number of data bytes supported is that the total number of bytes (including data bytes, parity bytes, and the added zero bytes of the

last short code word) is equal to 65535 in 8 bit input, 65534 in 16 bit input, and 65532 in 32 bit input. When specifying the number of data bytes you want to process, the number can be any value within the supported range for 8 bit input. For 16 bit input, the number can only be the even numbers within the supported range. For 32 bit input, the number can only be those which is a multiple of 4 within the supported range.

DATA_IN

Thirty-two bit input, the data sequence to be encoded. When mode is set to "00", only the 8 msb is used as input. When mode is set to "01", only the 16 msb is used as input. When mode is set to "10" or "11", the full 32 bit is used as input. The first data symbol (1-byte, 2-byte, or 4-byte) of the data sequence should be one clock after the START pulse. The encoder will read in one data symbol per clock. For every 239 data symbols, the encoder will need 16 clock cycles to add the parity bytes. If the last part of the data sequence is less than 239 data symbols, the encoder will add some zeros to the last code word and calculate the parity bytes. In the output, the added zeros will be trimmed off as specified in the GPON (G.984.3) standard.

CODE_OUT

Thirty-two bit output, the output code word. When mode is set to "00", only the 8 msb is the output. When mode is set to "01", only the 16 msb is the output. When mode is set

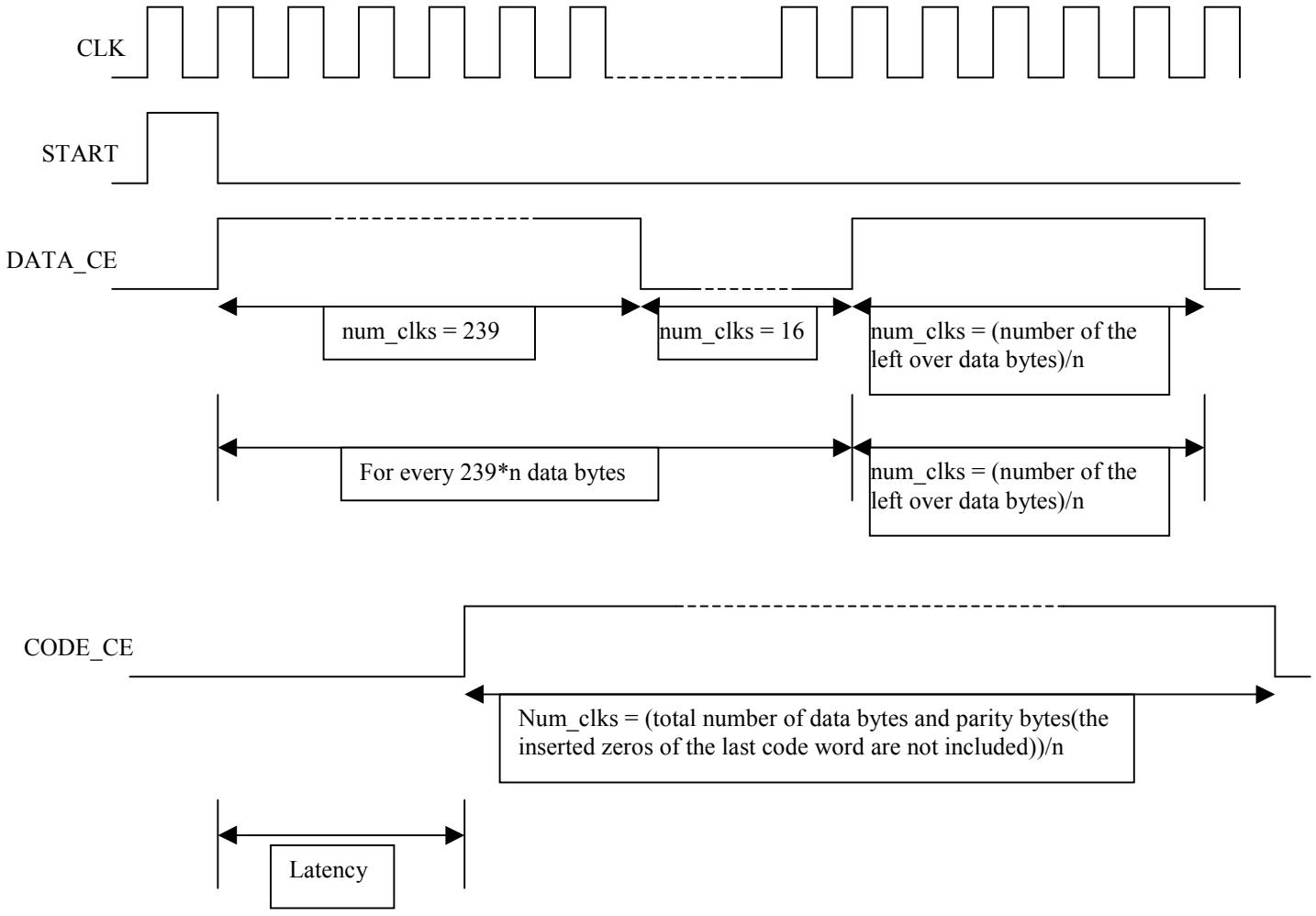

Figure 3. Timing Diagram of the GPON FEC Encoder

to “10” or “11”, the full 32 bit is the output. CODE_OUT is a continuous code word stream. Even for the last short code word there is no gap between the data bytes and the parity bytes.

CODE_CE
One bit output, the clock enable for outputting the code word. CODE_CE is used to enable the clock for the next processing module of the code word.

Timing Diagram

The GPON FEC encoder is very easy to be integrated into a larger design. Figure 3 helps to clarify some of the synchronization issues, where DATA_CE labels when the data should be fed into the encoder, and n = 1 when mode = “00”, n = 2 when mode = “01”, and n = 4 when mode = “10” or “11”.

Following the START pulse, the data is fed into the encoder one data symbol (1 byte, 2 byte or 4 byte) per clock. For every 239 data symbols, the encoder will need 16 clock cycles to append the parity bytes. After the 16 clock cycles, another 239 data symbols is fed into the encoder followed by 16 clock cycles, and so on. For the last part of the data sequence, no matter if it is 239 data symbols or less, it is simply fed into the encoder. The encoder will handle the last short code word according to the GPON standard.

The output from the encoder is a continuous code word stream. There is no gap between the data bytes and the parity bytes of the last short code word. The added zeros of the last short code word are already trimmed off. CODE_CE is used to enable the clock for the next processing module of the code word.

The latency of the encoder is 263 clock cycles.

Deliverables

Deliverables include the encoder/decoder and the test bench. For Xilinx FPGA implementation, both source code and netlist are available. For ASIC implementation, only source code will be delivered. Source code can be in VHDL or Verilog.

Ordering Information

We have flexible licensing structures. Please use the following information to contact us:

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