(973, 935) Reed-Solomon Decoder

Features

- **10 bit symbol, (n, k) = (973, 935) Reed-Solomon decoder**
- **Available for FPGA or ASIC implementation**
- **High speed design, maximum clock speed reaches 140 MHz, throughput reaches 1.4 Gbps in Virtex II, higher in ASIC**
- **Compact design, uses 1897 CLB slices and 5 Block Rams in Virtex II, among the smallest on the market**
- **Can work continuously with no gap between code blocks**
- **Detect number of received blocks**
- **Detect number of corrected errors**
- **Detect number of detected errors**
- **Fully synchronous one clock design**
- **Minimum latency is 973 + 886 clock cycles, maximum latency is 973 + 1076 clock cycles, depending on the maximum number of detectable errors. For continuous operation, maximum latency is 973+971 clock cycles, and maximum number of detectable symbol errors is 24.**

Functional Description

The decoder has three functional blocks and one memory block as shown in Figure 1. First the syndrome unit calculates the syndromes. Then the key equation solver solves the key equation for the error location polynomial. The correction unit calculates the error location and value and then adds the error sequence to the received code word to get the corrected code word. The memory unit is used to store the received code word while the decoder calculates the syndromes and solves the key equation. During the correction stage, the stored code word is read out from the memory and added to the error sequence to get the corrected code word.

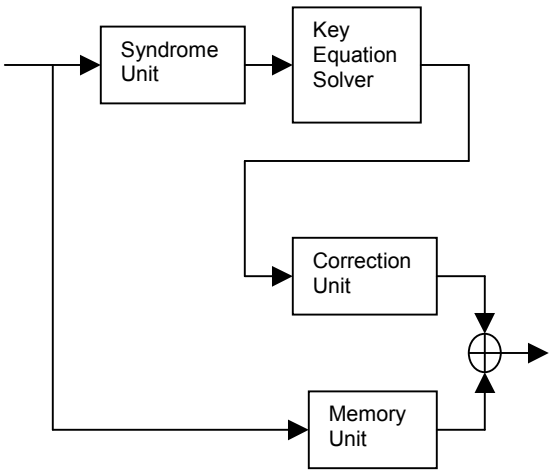

Figure 1. Block diagram of the Reed-Solomon decoder.

Pin Out

Figure 2 is the schematic symbol of the Reed-Solomon decoder.

RST

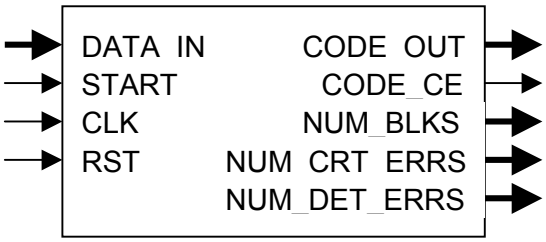

Figure 2. Schematic symbol of the decoder

One bit input, the asynchronous reset. When RST is set high, all the internal flip-flops are asynchronously initialized. The core will stay in this state until RST is set low.

CLK

One bit input, the global clock. All sequential logic acts on the rising edge of CLK.

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START
One bit input, the signal to start the decoding process. At the rising edge of CLK, if START is high while RST is low, the internal state machine will start the decoding process. For continuous operation, the START signal for the next code block must line up with the last symbol of the previous code block. Otherwise, the START signal must leave enough space for the decoder to finish the decoding of the previous code block. The length of START should be one clock cycle.

DATA_IN
Ten bit input, the received code word. The first symbol of the code word should be one clock after the START pulse. The decoder reads in one symbol every clock. Each code word must have 973 symbols with 935 data symbols and 38 parity check symbols. If there is a second code word following the first one, the second code word must follow the first one either with no gap or with a five-clock cycle gap.

CODE_OUT
Ten bit output, the decoded code word. If there are nineteen or less than nineteen erroneous symbols, the output is the corrected code word. Otherwise, the output is unpredictable.

CODE_CE
One bit output, the clock enable for outputting the corrected code word. The length of CODE_CE is 973 clock cycles.

NUM_BLKS
Fifteen bit output, the number of received blocks so far. Only RST can set this signal to zero.

NUM_CRT_ERRS
Fifteen bit output, the number of corrected symbol errors so far. Only RST can set this signal to zero.

NUM_DET_ERRS
Fifteen bit output, the number of detected symbol errors so far. Only RST can set this signal to zero.

Timing Diagrams

The Reed-Solomon decoder is very easy to be integrated into a larger design. The following timing diagrams help to clarify some of the synchronization issues.

Figure 3 shows the timing diagram at the starting point of the decoding process, where D0 is the first symbol of the received code word.

Figure 4 shows the timing diagram at the starting point of the output, where C0 is the first symbol of the decoded code word.

Figure 5 shows the timing diagram of the continuous operation mode, where DA972 is the last symbol of the first received code word and DB0 is the first symbol of the following code word.

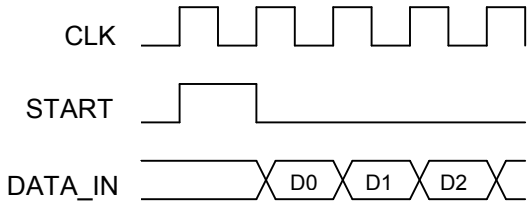

Figure 3. The timing diagram at the starting point of the decoding process

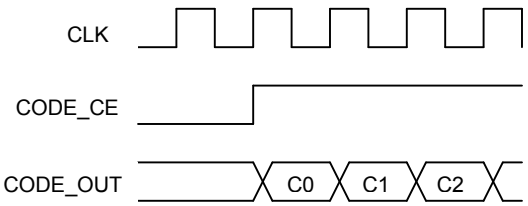

Figure 4. The timing diagram at the starting point of the output

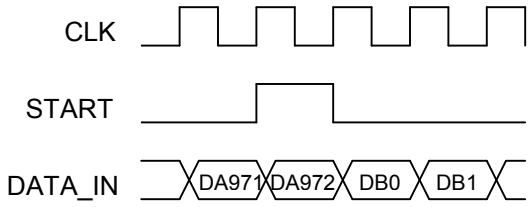

Figure 5. The timing diagram of the continuous operation mode

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Deliverables

Deliverables include the encoder/decoder and the test bench. For FPGA implementation, both source code and netlist are available. For ASIC implementation, only source code will be delivered. Source code can be in VHDL or Verilog.

Ordering Information

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