

## (973, 935) Reed-Solomon Encoder

### Features

- 10 bit symbol,  $(n, k) = (973, 935)$  Reed-Solomon Encoder
- Available for FPGA or ASIC implementation
- High speed design, maximum clock speed reaches 200 MHz, throughput reaches 2 Gbps in Virtex II, higher in ASIC
- Compact design, uses 480 CLB slices in Virtex II, among the smallest on the market
- Can work continuously with no gap between code blocks
- Fully synchronous one clock design
- One clock cycle latency

### Functional Description

The block diagram of the encoder is shown in Figure 1. The major functional block of the encoder is the parity unit. While the encoder outputs the data symbol, the parity unit calculates the parity symbol at the same time. The parity symbols are appended at the end of the data block to form the whole code word.

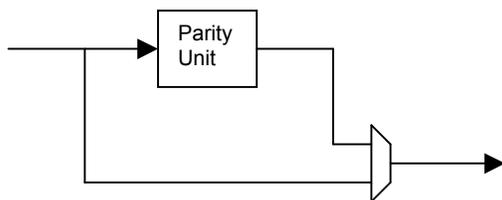


Figure 1. Block diagram of the Reed-Solomon encoder.

### Pin Out

Figure 2 is the schematic symbol of the Reed-Solomon encoder.

#### RST

One bit input, the asynchronous reset. When RST is set high, all the internal flip-flops are asynchronously initialized. The core will stay in this state until RST is set low.

#### CLK

One bit input, the global clock. All sequential logic acts on the rising edge of CLK.

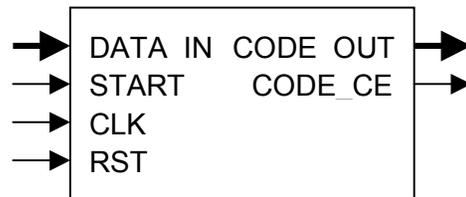


Figure 2. Schematic symbol of the encoder

#### START

One bit input, the signal to start the encoding process. At the rising edge of CLK, if START is high while RST is low, the internal state machine will start the encoding process. For continuous operation, the START signal for the next code block must line up with the last parity symbol of the previous code block. Otherwise, the START signal must leave enough space for the decoder to finish the decoding of the previous code block. The length of START should be one clock cycle.

#### DATA\_IN

Ten bit input, the data block to be encoded. The first symbol of the data block should be one clock after the START pulse. The encoder reads in one symbol every clock. Each data block must have 935 symbols and the encoder will append 38 parity check symbols at the end of the data block. For continuous operation, there must be a 38-clock cycle gap between the last DATA symbol of the first data block and the first DATA symbol of the following data block. Otherwise, there must be enough space for the decoder to finish the decoding of the previous code block.

**CODE\_OUT**

Ten bit output, the output code word. The first 935 symbols are the data block. The following 38 symbols are the parity symbols.

**CODE\_CE**

One bit output, the clock enable for outputting the code word. The length of CODE\_CE is 973 clock cycles.

**Timing Diagrams**

The Reed-Solomon encoder is very easy to be integrated into a larger design. The following timing diagrams help to clarify some of the synchronization issues.

Figure 3 shows the timing diagram at the starting point of the encoding process, where D0 is the first symbol of the data sequence.

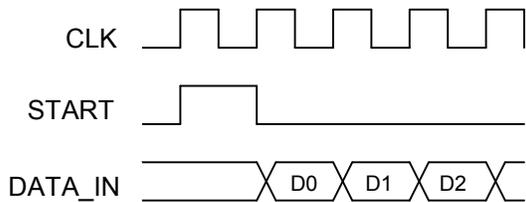


Figure 3. The timing diagram at the starting point of the encoding process

Figure 4 shows the timing diagram at the starting point of the output, where C0 is the first symbol of the code word.

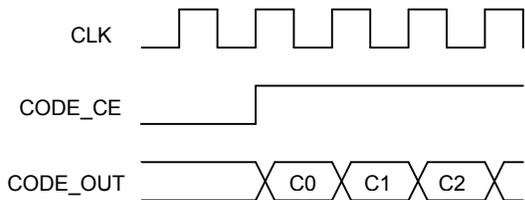


Figure 4. The timing diagram at the starting point of the output

Figure 5 shows the timing diagram of the continuous operation mode, where DA972 is

the last parity symbol of the first code word and DB0 is the first symbol of the following data sequence word.

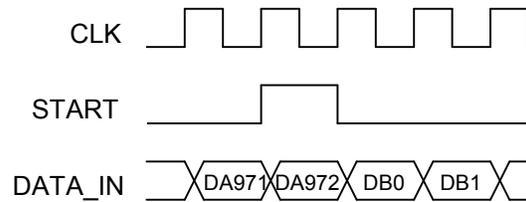


Figure 5. The timing diagram of the continuous operation mode

**Deliverables**

Deliverables include the encoder/decoder and the test bench. For FPGA implementation, both source code and netlist are available. For ASIC implementation, only source code will be delivered. Source code can be in VHDL or Verilog.

**Ordering Information**

We have flexible licensing structures. Please use the following information to contact us:

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