High Throughput Flexible Reed-Solomon Decoder

Features

- **Flexible Reed-Solomon decoder, number of parity check bytes can be 2, 4, 6, …, 16, code length and data length can be any value only if they satisfy the basic requirements of Reed-Solomon codes**
- **Available for FPGA or ASIC implementation**
- **High speed design, low gate count version reaches 1.12 Gbps data rate and low latency version reaches 800 Mbps data rate in Virtex II, higher in ASIC**
- **Compact design, low gate count version uses 1162 CLB slices and low latency version uses 1581 CLB slices in Virtex II, among the smallest on the market**
- **Code length and data length can change from block to block**
- **Fully synchronous one clock design**
- **Code length + 11 * t + 9 clock cycle latency in low latency version**
- **Code length + 2 * (t^2) + 8 * t + 12 clock cycle latency in low gate count version**

Functional Description

The decoder has three functional blocks and one memory block as shown in Figure 1. First the syndrome unit calculates the syndromes. Then the key equation solver solves the key equation for the error location polynomial. The correction unit calculates the error location and value and then adds the error sequence to the received code word to get the corrected code word. The memory unit is used to store the received code word while the decoder calculates the syndromes and solves the key equation. During the correction stage, the stored code word is read out from the memory and added to the error sequence to get the corrected code word.

Pin Out

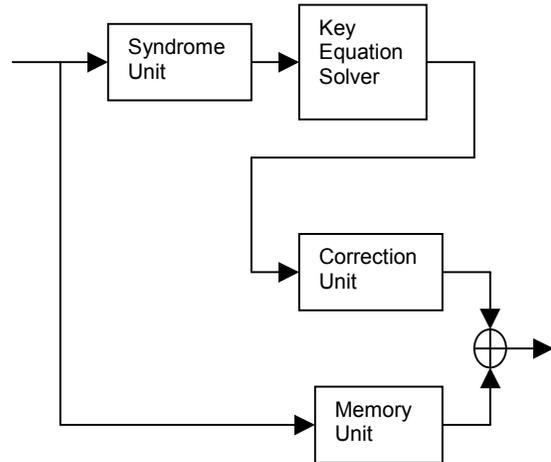Figure 2 is the schematic symbol of the Reed-Solomon decoder.
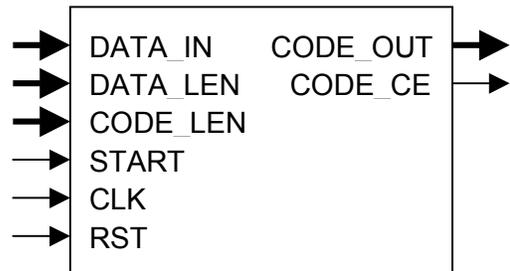

Figure 1. Block diagram of the Reed-Solomon decoder.

Figure 2. Schematic symbol of the decoder

RST
One bit input, the asynchronous reset. When RST is set high, all the internal flip-flops are asynchronously initialized. The core will stay in this state until RST is set low.

CLK
One bit input, the global clock. All sequential logic acts on the rising edge of CLK.

START

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One bit input, the signal to start the decoding process. At the rising edge of CLK, if START is high while RST is low, the internal state machine will start the decoding process. The length of START should be one clock cycle.

CODE_LEN
Eight bit input, the code length. The code length can be any value only if it satisfies the basic requirements of Reed-Solomon codes.

DATA_LEN
Eight bit input, the data length The data length can be any value only if it satisfies the basic requirements of Reed-Solomon codes.

DATA_IN
Eight bit input, the received code word. The first byte of the code word should be one clock after the START pulse. The decoder reads in one byte every clock.

CODE_OUT
Eight bit output, the decoded code word. If the number of erroneous bytes is less than or equal to half the number of the parity check bytes, the output is the corrected code word. Otherwise, the output is unpredictable.

CODE_CE
One bit output, the clock enable for outputting the corrected code word. The length of CODE_CE is CODE_LEN clock cycles.

Timing Diagrams

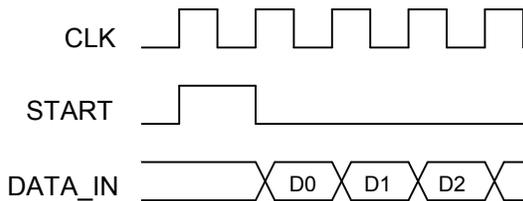The Reed-Solomon decoder is very easy to be integrated into a larger design. The following timing diagrams help to clarify some of the synchronization issues.

Figure 3 shows the timing diagram at the starting point of the decoding process, where D0 is the first byte of the received code word.
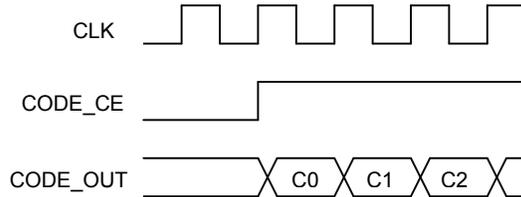

Figure 4. The timing diagram at the starting point of the output

Figure 4 shows the timing diagram at the starting point of the output, where C0 is the first byte of the decoded code word.

Deliverables

Deliverables include the encoder/decoder and the test bench. For Xilinx FPGA implementation, both source code and netlist are available. For ASIC implementation, only source code will be delivered. Source code can be in VHDL or Verilog.

Ordering Information

We have flexible licensing structures. Please use the following information to contact us:

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Figure 3. The timing diagram at the starting point of the encoding process