High Throughput Flexible Reed-Solomon Encoder

Features

- **Flexible Reed-Solomon encoder, number of parity check bytes can be 2, 4, 6, …, 16, code length and data length can be any value only if they satisfy the basic requirements of Reed-Solomon codes**
- **Available for FPGA or ASIC implementation**
- **High speed design, reaches 720 Mbps data rate in Virtex II, or 700Mbps in Spartan III, higher in ASIC**
- **Compact design, uses 642 CLB slices in Vietex II, or 631 CLB slices in Spartan III, among the smallest on the market**
- **Code length and data length can change from block to block**
- **Fully synchronous one clock design**
- **One clock cycle latency**

Functional Description

The block diagram of the encoder is shown in Figure 1. The major functional block of the encoder is the parity unit. While the encoder outputs the data symbol, the parity unit calculates the parity symbol at the same time. The parity symbols are appended at the end of the data block to form the whole code word.

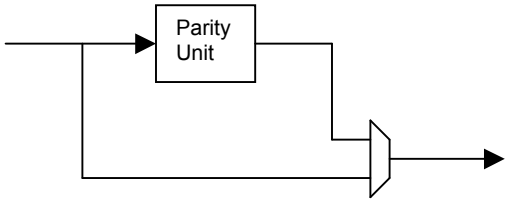

Figure 1. Block diagram of the Reed-Solomon encoder.

Pin Out

Figure 2 is the schematic symbol of the Reed-Solomon encoder.

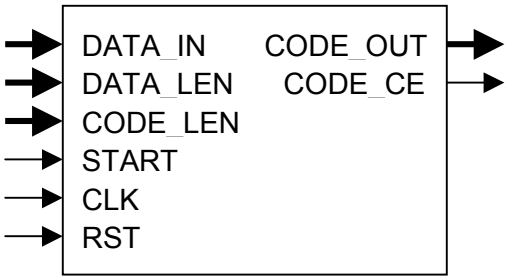

Figure 2. Schematic symbol of the encoder

RST

One bit input, the asynchronous reset. When RST is set high, all the internal flip-flops are asynchronously initialized. The core will stay in this state until RST is set low.

CLK

One bit input, the global clock. All sequential logic acts on the rising edge of CLK.

START

One bit input, the signal to start the encoding process. At the rising edge of CLK, if START is high while RST is low, the internal state machine will start the encoding process. The length of START should be one clock cycle.

CODE_LEN

Eight bit input, the code length. The code length can be any value only if it satisfies the basic requirements of Reed-Solomon codes.

DATA_LEN

Eight bit input, the data length. The data length can be any value only if it satisfies the basic requirements of Reed-Solomon codes.

DATA_IN

Eight bit input, the data sequence to be encoded. The first byte of the data sequence should be one clock after the START pulse. The encoder reads in one byte every clock. Each data sequence must be at least 1 byte long.

CODE_OUT
Eight bit output, the output code word. The first part of the code word is the data sequence and the second part is the parity check bytes.

CODE_CE
One bit output, the clock enable for outputting the code word. The length of CODE_CE equals CODE_LEN clock cycles.

Timing Diagrams

The Reed-Solomon encoder is very easy to be integrated into a larger design. The following timing diagrams help to clarify some of the synchronization issues.

Figure 3 shows the timing diagram at the starting point of the encoding process, where D0 is the first byte of the data sequence.

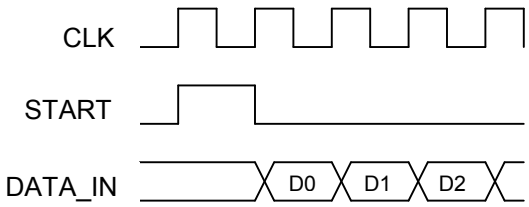

Figure 3. The timing diagram at the starting point of the encoding process

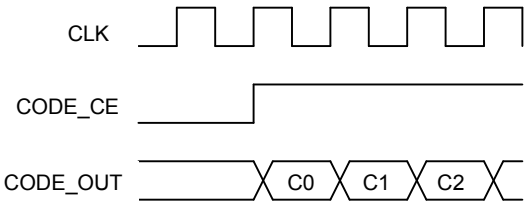

Figure 4. The timing diagram at the starting point of the output

Figure 4 shows the timing diagram at the starting point of the output, where C0 is the first byte of the code word.

Deliverables

Deliverables include the encoder/decoder and the test bench. For Xilinx FPGA implementation, both source code and netlist are available. For ASIC implementation, only source code will be delivered. Source code can be in VHDL or Verilog.

Ordering Information

We have flexible licensing structures. Please use the following information to contact us:

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