Viterbi Decoder

Features

- **Industry standard k = 7, (G0, G1) = (133, 171), rate ½ Viterbi decoder**
- **Available for Xilinx FPGA or ASIC implementation**
- **High speed design, reaches 122 Mbps data rate in Virtex II, or 108 Mbps data rate in Spartan III, higher in ASIC**
- **Compact design, uses 1168 CLB slices and 4 Block Rams in Virtex II, or 1236 CLB slices and 4 Block Rams in Spartan III, among the smallest on the market**
- **4 bit soft input**
- **Length 64 trace back**
- **Fully synchronous one clock design**
- **267 clock cycles latency**

Functional Description

The decoder has three functional blocks as shown in Figure 1. The branch metric unit calculates the branch metrics, the add compare select unit select the surviving branches based on the branch metrics, and the trace back unit generates the decoded data bit.

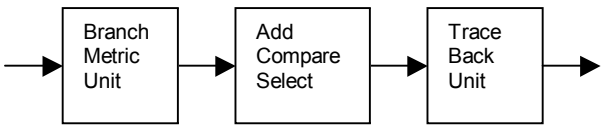

Figure 1. Block diagram of the Viterbi decoder.

Pin Out

Figure 2 is the schematic symbol of the Viterbi decoder.

RST
One bit input, the asynchronous reset. When RST is set high, all the internal flip-flops are asynchronously initialized. The core will stay in this state until RST is set low.

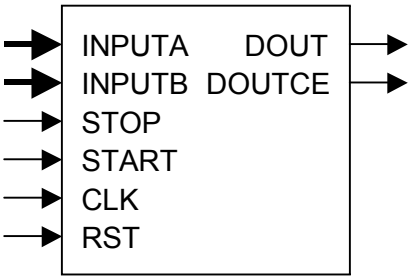

Figure 2. Schematic symbol of the decoder

CLK
One bit input, the global clock. All synchronous logic acts on the rising edge of CLK.

START
One bit input, the signal to start the decoding process. At the rising edge of CLK, if START is high while RST is low, the internal state machine will start the decoding process. The length of START should be one clock cycle. Once the decoding process is started, only STOP can synchronously and RST can asynchronously stop the decoding process.

STOP
One bit input, the signal to stop the decoding process. It is the designer's responsibility to determine when to stop the decoding process.

INPUTA
Four bit input, one of the two received data inputs. The first input data symbol should one clock behind START. The four bit soft input is chosen based on the compromise of the performance and the complexity of the design. Higher resolution input doesn't justify the complexity increase in the design.

INPUTB

Four bit input, one of the two received data inputs. The first input data symbol should one clock behind START. The four bit soft input is chosen based on the compromise of the performance and the complexity of the design. Higher resolution input doesn't justify the complexity increase in the design.

DOUT
One bit output, the decoded data bit. There is one decoded data bit for every clock.

DOUTCE
One bit output, the clock enable for outputting the decoded data.

Timing Diagrams

The Viterbi decoder is very easy to be integrated into a larger design. The following timing diagrams help clarify some of the synchronous issues.

Figure 3 shows the timing diagram at the starting point of the decoding process, where (A0, B0) is the first data symbol of the received code.

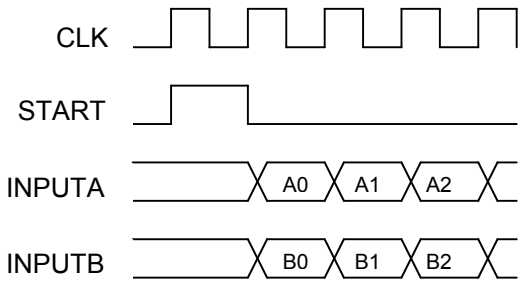

Figure 3. The timing diagram at the starting point of the decoding process

Figure 4 shows the timing diagram at the starting point of the output, where C0 is the first decoded output bit.

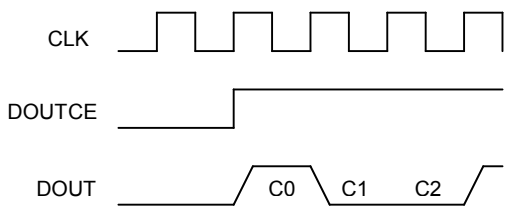

Figure 4. The timing diagram at the starting point of the output

Deliverables

Deliverables include the convolutional encoder, the Viterbi decoder and the test bench. For Xilinx FPGA implementation, both source code and netlist are available. For ASIC implementation, only source code will be delivered. Source code can be in VHDL or Verilog.

Ordering Information

We have flexible licensing structures. Please contact our local distributors or use the following information to contact us directly:

Highland Communications Technologies
225 Bowen Road, Fort Erie
Ontario, Canada L2A 2Y6

Tel: 1-905-658-0989
Fax: 1-905-871-2096
Email: sales@highlandcomm.com

Web site:
http://www.highlandcomm.com/